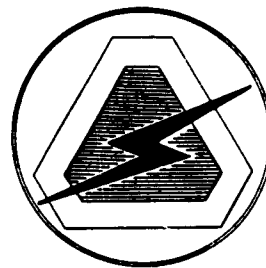# A METHOD OF BASIC TEMPERATURE COMPENSATION IN TRANSISTORS

Richard L. Brayden

MAY 8 1963

February 1963

UNITED STATES ARMY
ELECTRONICS RESEARCH AND DEVELOPMENT LABORATORY

FORT MONMOUTH, N.J.

U. S. ARMY ELECTRONICS RESEARCH AND DEVELOPMENT LABORATORY
FORT MONMOUTH, NEW JERSEY

February 1963

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A METHOD OF BASIC TEMPERATURE COMPENSATION IN TRANSISTORS

Richard L. Brayden

DA Task Nr. 3A99-21-003-01

ABSTRACT

A semiconductor device complex, consisting of a diode-transistor combination, that effectively compensates for normal transistor gain variations as a function of temperature has been developed under Signal Corps Contract DA 36-039 SC-87276, Hoffman Electronics Corporation. This device has the characteristics of the normal transistor, except that in the range of 0°C to 70°C the h_{FE} changes by less than 10%. The complex device is in a single transistor package and may be treated circuit-wise as if it were an ordinary NPN silicon transistor.

In this report a direct comparison is made between the new device and an electronically similar commercially available transistor. In addition, a simple technique called m-slope analysis is presented that gives a method of pinpointing the dominant leakage effects in both planar and mesa transistors and to what extent these effects occur.

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GLOSSARY

h_{FE}	D.C. current gain
S	Surface recombination velocity
P_N	Hole concentration in emitter region
D_N	Diffusion constant of electrons in base region
L_B	Diffusion length of electrons in base region
W_D	Width of depletion layer
W	Base width
A	Cross-sectional area of the conduction path
V_E	Emitter Base Voltage
q	1.6×10^{-19} coulomb
k	1.38×10^{-23} watt sec/$^{\circ}$C
τ_{po}	Lifetime for holes injected into highly n-type specimen
τ_{no}	Lifetime for electrons injected into highly p-type specimen
T	Temperature in $^{\circ}$k
A_S	Effective surface area for recombination
W_E	Width of emitter region
D_p	Diffusion constant of holes in emitter region
N_p	Electron concentration in base region
n_i	Intrinsic concentration

A METHOD OF BASIC TEMPERATURE COMPENSATION IN TRANSISTORS

INTRODUCTION

The problem of the variation of a transistor's parameters with temperature has long been a serious one for circuit designers and has led to extensive circuit manipulations in an attempt to reduce the effects of these variations on a system's performance. Because of this, a contract was awarded to the Hoffman Electronics Corporation[1] to study this problem. The specific objectives of this contract were:

    1. to make a thorough study of the problem of designing a temperature insensitive transistor.

    2. to fabricate practical transistors that would have less than 10 percent current-gain variation between 0°C and 70°C.

This report is an evaluation of the experimental transistor models that were submitted at the end of the contract to support the theory developed under the contract.

DISCUSSION

One of the major contributions of this contract was the development of a simple analytical tool called m-slope analysis. With this analytical technique it was possible to pinpoint which leakage effects were dominant in both a double-diffused mesa and a planar transistor.

For a complete understanding of this analytical technique the following derivation is offered.

M-slope Analysis

The original starting point of this analysis was the Webster equation for dc current gain. During the course of the contract, two additional terms were added to the Webster equation which accounted for the effects of emitter space-charge recombination and surface leakage. The complete expression for the current gain of a transistor was shown to be:

$$\frac{1}{h_{FE}} = \left[\left(\frac{1}{h_{FE}}\right)_S + \left(\frac{1}{h_{FE}}\right)_E + \left(\frac{1}{h_{FE}}\right)_{SP} + \left(\frac{1}{h_{FE}}\right)_B + \left(\frac{1}{h_{FE}}\right)_L\right] \tag{1}$$

where

$\left(\frac{1}{h_{FE}}\right)_S$ . . . . surface term

$\left(\frac{1}{h_{FE}}\right)_E$ . . . . emitter efficiency term

$\left(\frac{1}{h_{FE}}\right)_{SP}$ . . . . space charge recombination term

1

$\left(\dfrac{1}{h_{FE}}\right) B$ . . . . bulk recombination term

$\left(\dfrac{1}{h_{FE}}\right) L$ . . . . Cutler-Bath
surface leakage term.

Equation (1) can also be expressed as

$$\frac{1}{h_{FE}} = \frac{(I_B)_S + (I_B)_E + (I_B)_{SP} + (I_B)_B + (I_B)_L}{I_C} \tag{2}$$

where

I_C = collector current

$(I_B)_i$ = base current components due to the various effects
(i = S, E, SP, B, L).

The collector current I_C and the various base current components $(I_B)_i$ depend on the _dimensionless quantity_, V,

where $V = \dfrac{qV_E}{kT}$

and $\quad I_C = A_1 \exp V \tag{3}$

where

$$A_1 = \frac{qN_P D_N}{W} \tag{4}$$

$(I_B)_S = \quad A_2 \exp V \tag{5}$

where

$$A_2 = \frac{SWA_S}{D_N A} A_1 \tag{6}$$

$(I_B)_E = A_3 \exp V \tag{7}$

where

$$A_3 = \frac{qP_N D_P}{W_E} \tag{8}$$

$(IB)_{SP} = A_4 \exp \dfrac{V}{2} \tag{9}$

where

$$A_4 = \frac{qN_i W_d}{(\tau_{po} + \tau_{no})} \tag{10}$$

$(I_B)_B = A_5 \exp V \tag{11}$

2

where
$$A_5 = \frac{1}{2}\left(\frac{W}{L_B}\right)^2 A_1 \tag{12}$$

$$(I_B)_L = A_6 \exp \frac{V}{2} + \left[A_7 - A_8 \exp - \frac{V_E}{2}\right]^*, \tag{13}$$

where
$$A_6 = L \left(2\sigma\frac{kT}{q} \, J^1_{DO}\right)^{\frac{1}{2}} \tag{14}$$

$$A_7 = A_6 \left(\frac{J^1_{ORG}}{J^1_{DO}}\right) \tag{15}$$

$$A_8 = \frac{1}{2}\left[\frac{J^1_{ORG}}{J^1_{DO}} - C_1\right] \tag{16}$$

also
$$A_6 \exp \frac{V}{2} \gg \left[A_7 - A_8 \exp - \frac{V}{2}\right]. \tag{17}$$

The total base current is

$$(I_B) \text{ total} = \left[(I_B)_S + (I_B)_E + (I_B)_{SP} + (I_B)_B + (I_B)_L\right]. \tag{18}$$

By substituting equations (5), (7), (9), (11), (13) in equation (18), the following equation is attained:

$$(I_B) \text{ total} = \left[(A_2 + A_3 + A_5) \exp V + (A_4 + A_6) \exp \frac{V}{2} + A_7 - A_8 \exp - \frac{V}{2}\right] \tag{19}$$

or
$$(I_B)_{total} = B_2 \exp \frac{V}{2} + B_3 \exp V + \left[A_7 - A_8 \exp - \frac{V}{2}\right] \tag{20}$$

where
$$B_2 = A_4 + A_6$$
$$B_3 = A_2 + A_3 + A_5. \tag{21}$$

Equation (20) can be expressed by an equation of the form

$$(I_B)_{total} = B_1 \exp \frac{V}{m} \tag{22}$$

where the value of m is related to the particular mechanism contributing to the base current in the voltage range under consideration.

---

* Derivation of this equation can be found in the 3rd Quarterly Report, Signal Corps Contract DA 36-039, SC-87276, Hoffman Electronics Corporation, pp. 2-17.

Therefore,

$$B_1 \exp \frac{V}{m} = B_2 \exp \frac{V}{2} + B_3 \exp V$$
$$+ \left[A_7 - A_8 \exp{-\frac{V}{2}} \right]. \tag{23}$$

Neglecting the small term of equation (23)

$$B_1 \exp \frac{V}{m} \approx B_2 \exp \frac{V}{2} + B_3 \exp V . \tag{24}$$

Equation (24) contains the constant unknown factor B_1. To solve this equation for the slope constant m, a second equation is needed. This equation can be obtained by differentiation of equation (24).

$$\frac{1}{m} \left[1 - \frac{V}{m} \frac{\partial m}{\partial v} \right] B_1 \exp \frac{V}{m} \approx \frac{B_2}{2} \exp \frac{V}{2}$$
$$+ B_3 \exp V. \tag{25}$$

Using equation (24) and (25) to eliminate the unknown factor, B_1,

$$\frac{1}{m} \left[1 - \frac{V}{m} \frac{\partial m}{\partial v} \right] \approx \frac{\frac{1}{2} \frac{B_2}{B_3} + \exp \frac{V}{2}}{\frac{B_2}{B_3} + \exp \frac{V}{2}} . \tag{26}$$

Assuming m is independent or almost independent of V, equation (26) becomes:

$$\frac{1}{m} \approx \frac{\frac{1}{2} \frac{B_2}{B_3} + \exp \frac{V}{2}}{\frac{B_2}{B_3} + \exp \frac{V}{2}} . \tag{27}$$

The term $B_2 \exp \frac{V}{2}$ represents the base current caused by surface leakage and space-charge recombination, and the term $B_3 \exp V$ is the base current caused by surface recombination, bulk recombination and the majority carrier flow into the emitter. The ratio of both current components characterizes the kind of base current.

$$\eta = \frac{B_2 \exp \frac{V}{2}}{B_3 \exp V} = \frac{B_2}{B_3} \exp -\frac{V}{2} \tag{28}$$

or

$$\frac{B_2}{B_3} = \eta \exp \frac{V}{2} . \tag{29}$$

Substituting equation (29) into equation (27) gives a simple expression for m:

$$\frac{1}{m} \approx \frac{\frac{1}{2} \eta + 1}{\eta + 1}$$

or

$$m \approx \frac{\eta + 1}{\frac{\eta + 1}{2}} \ .$$

The slope constant m is plotted as a function of η in Fig. 9.

At once a method of isolating which surface effects are predominant in a given transistor suggests itself. If the values of m are plotted on Fig. 9 for different current levels the η values are readily obtainable. If η is less than one, the major effect is surface recombination at high current levels and emitter space-charge recombination at low current levels. If the values of η are greater than one, the major effect is surface leakage at high current levels and emitter space-charge recombination at low current levels. This technique of analysis could be extremely valuable in analyzing surface passivization techniques on transistors and could prove a useful tool in both research and production control.

Fig. 10 shows the average values of m plotted for planar and mesa structures at both high and low values of current. It is seen that in planar devices, surface recombination plays a dominant role in the variation of h_{FE} (dc current gain) at high current levels; while at low current levels, surface recombination and emitter space-charge recombination are both important, with emitter space-charge recombination becoming more important as the current is reduced to still lower values.

In the double-diffused mesa transistor, Cutler-Bath leakage current is the dominant cause of temperature-gain variation. At very low current levels, a combination of both the Cutler-Bath leakage current and emitter space-charge recombination current becomes important, with the emitter space-charge recombination current gradually becoming the dominant factor as the current level is still further reduced.

Technique of Compensation

It has long been known that planar transistors have a greater temperature-gain variation than geometrically equivalent mesa structures. The reason for this, it was found, is that mesa transistors have a greater amount of leakage current than planar types, and this extra leakage current serves to control the temperature-gain variation of the mesa transistor. Also, because of the inherently excessive amounts of leakage current, mesa transistors have overall lower current gains than equivalent planar types. Utilizing this conclusion, it seemed apparent that the solution for controlling the current gain of a planar transistor would lie in introducing a controlled leakage path in the transistor.

The approach used to create this leakage path was the inclusion of a diode between the emitter and base of an ordinary, medium-power NPN silicon planar transistor. The effect of this diode would be to divert some of the base current of the transistor, thereby effectively lowering the current gain. This shunting effect would become increasingly predominant as the temperature increased so as to offset the inherent increase

in gain of the transistor. Since the inclusion of this diode would effectively reduce the actual current gain of the transistor, as well as control the gain, special high gain transistor units were produced so that when the diode was introduced the overall current gain of the transistor would be a reasonable value. The actual photographs of the physical structure of the experimental transistors, along with a pictorial view, are shown in Figs. 7 and 8.

Experimental Results

Upon receiving the experimental transistor models, the dc current gain was monitored over a temperature range of -25°C to 100°C. Although the initial specification called for no more than a ten percent variation of h_{FE} over the range of 0°C to 70°C, experiments were conducted to observe how these transistors performed beyond the temperature limits imposed by the original specifications. Figs. 1 and 2 show the variation of h_{FE} for two of these experimental devices at various values of collector current. As a control, a 2N702 transistor was selected to show the temperature-gain variation of a similar type of commercially available transistor. Fig. 3 shows the temperature gain variation of the 2N702 at different values of collector current. Next, the normalized current gain versus temperature (Figs. 4, 5 and 6) were plotted for all three units. For these normalized curves only the normalized current gains for the two extreme values of collector current were used. This was done because normalized values of current gain for the in-between values of collector current lie somewhere between the normalized gains of the highest value of collector current used and the lowest value of collector current used. It can be seen from these normalized curves that the experimental transistors offer an improvement in gain control of about 150%. Also, the experimental models offer better than the ten percent compensation called for by the original specifications.

CONCLUSION

The final conclusion of this study is that gain compensation in transistors is indeed possible and that, with a further understanding of the transistor structure and better methods of building and controlling surfaces, high gain temperature-compensated devices over wide current ranges will become possible.

REFERENCE

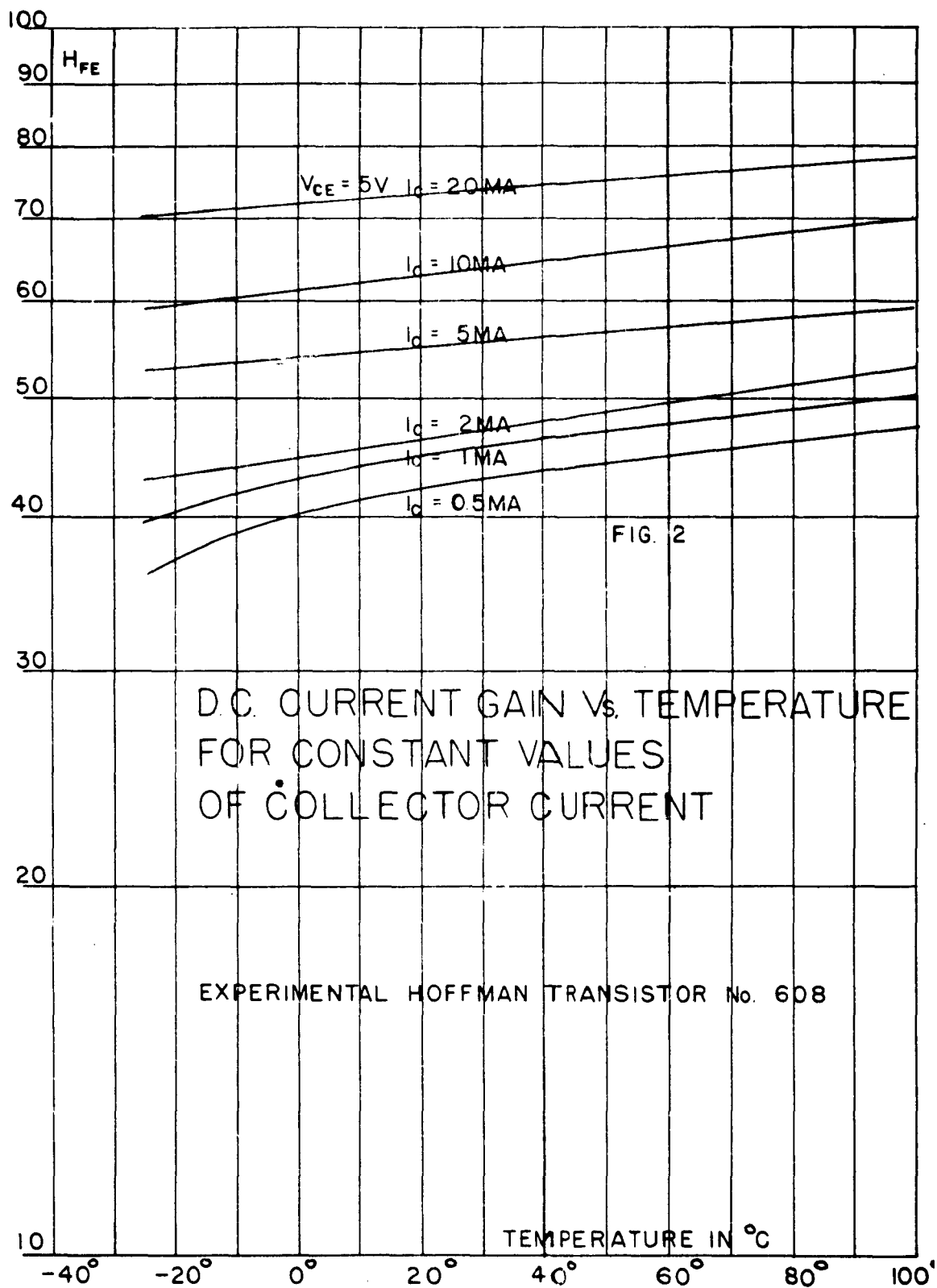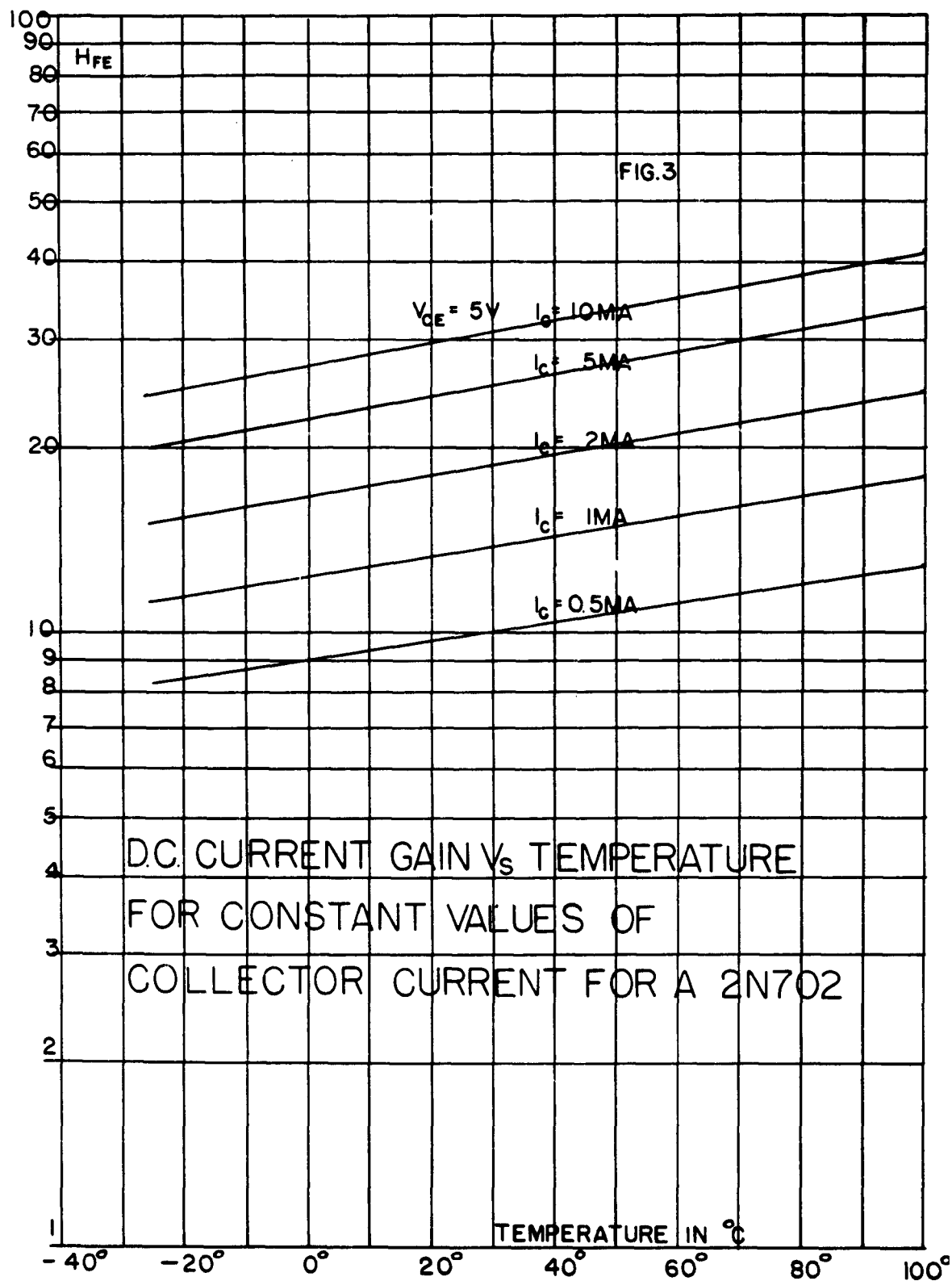1. USAELRDL Contract DA 36-039 SC-87276, "Temperature Insensitive Transistor," May 1961-May 1962.
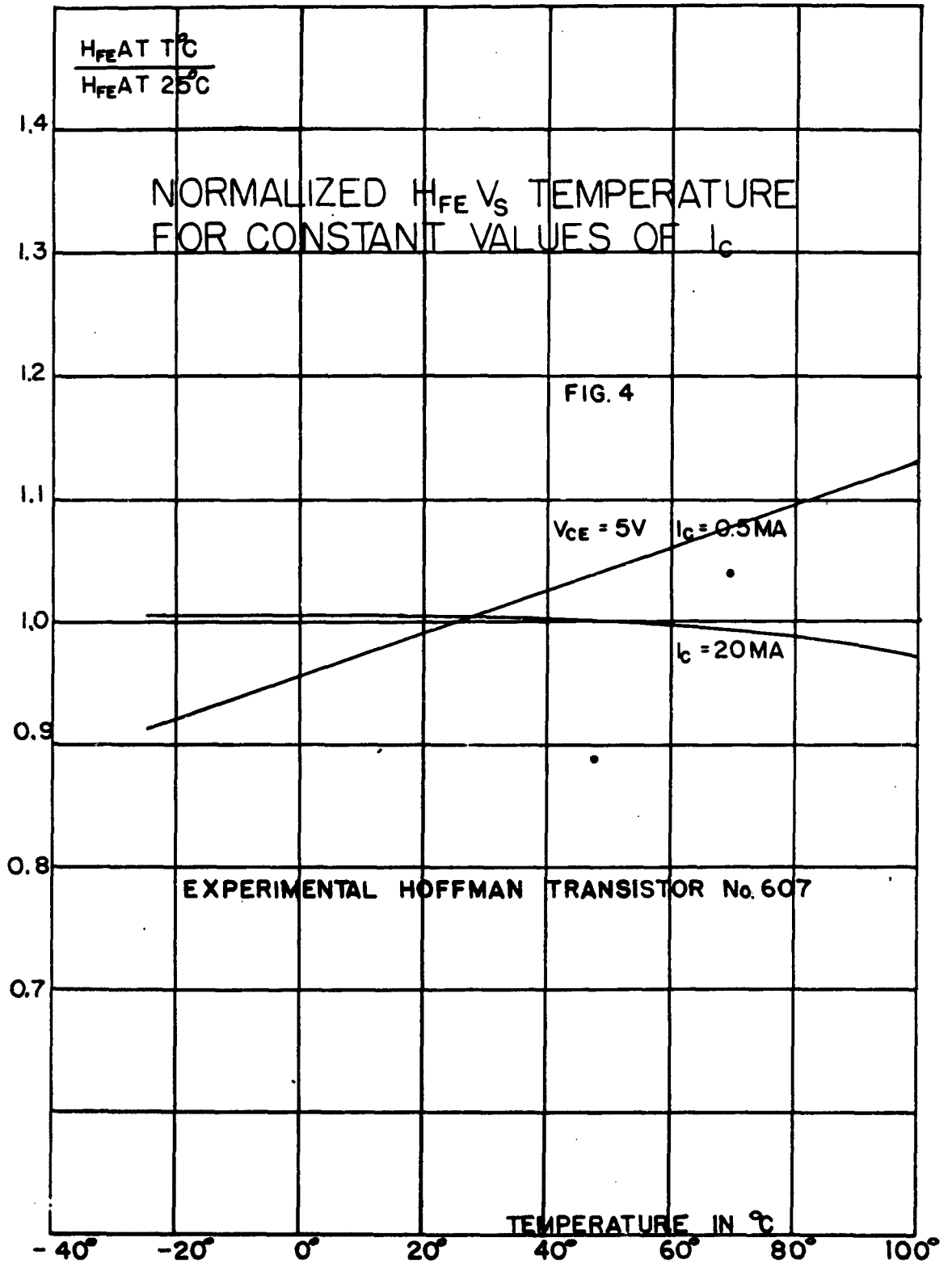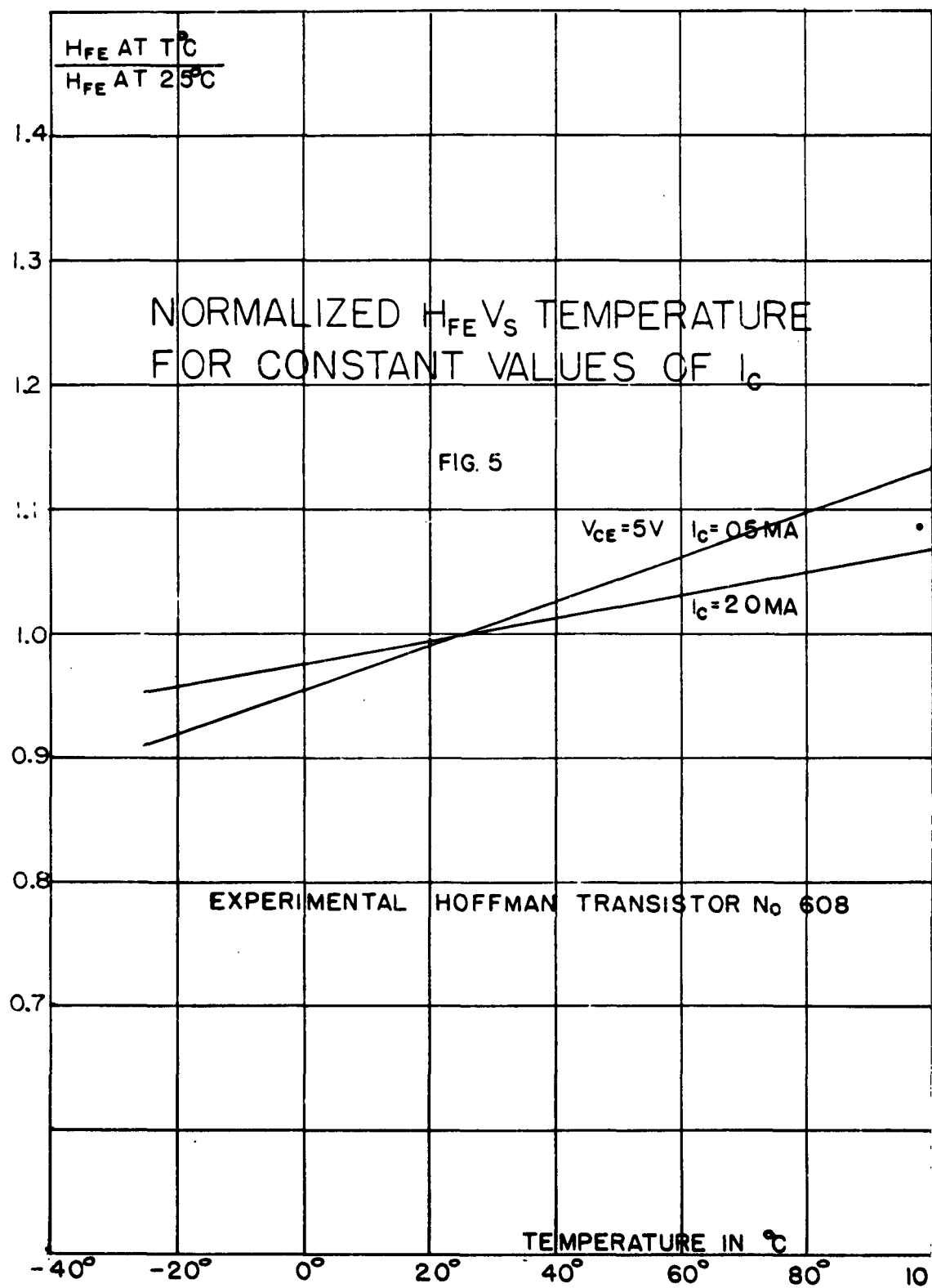
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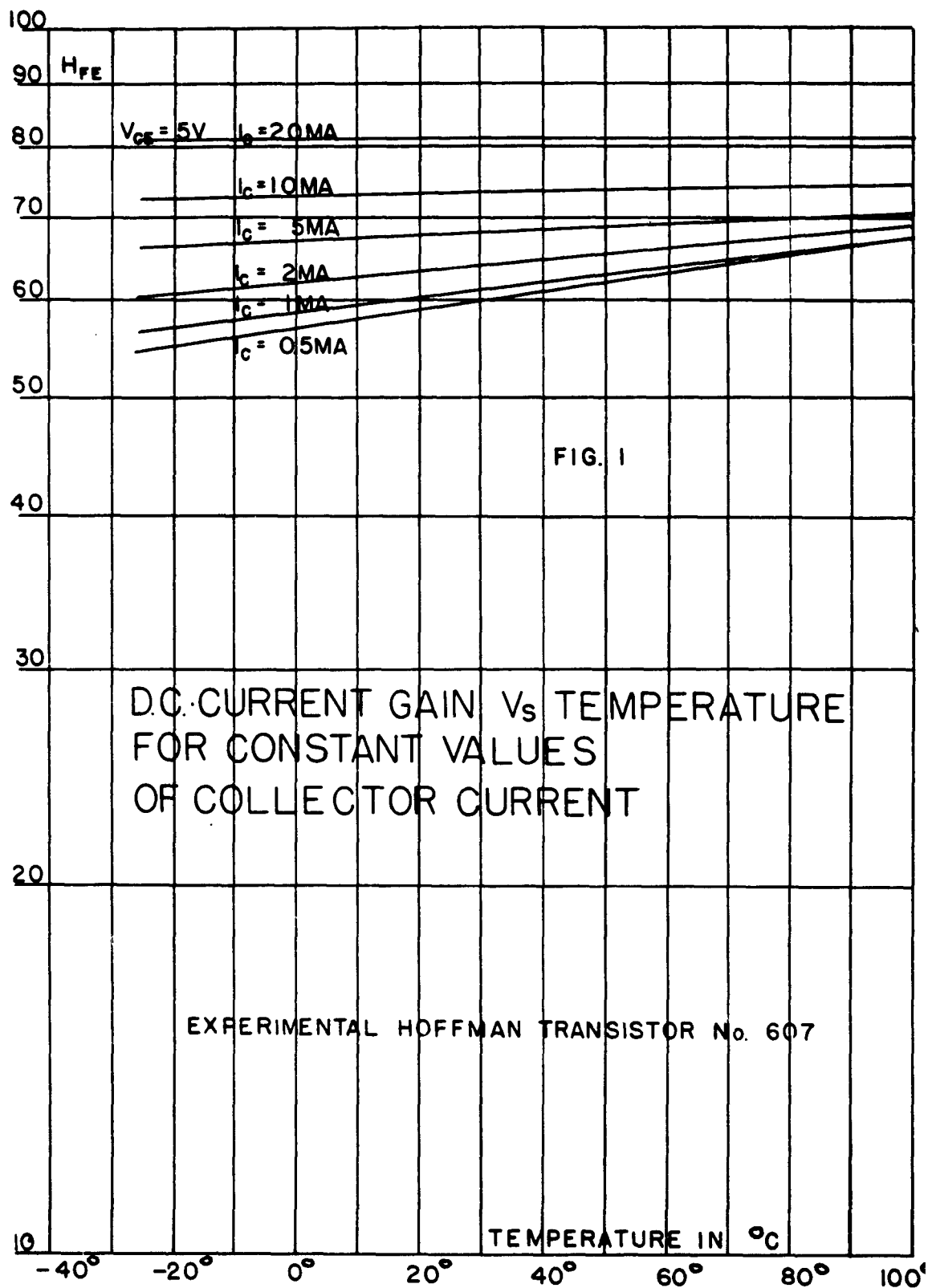
D.C. CURRENT GAIN Vs TEMPERATURE
FOR CONSTANT VALUES
OF COLLECTOR CURRENT

EXPERIMENTAL HOFFMAN TRANSISTOR No. 607

7

100

90 H_{FE}
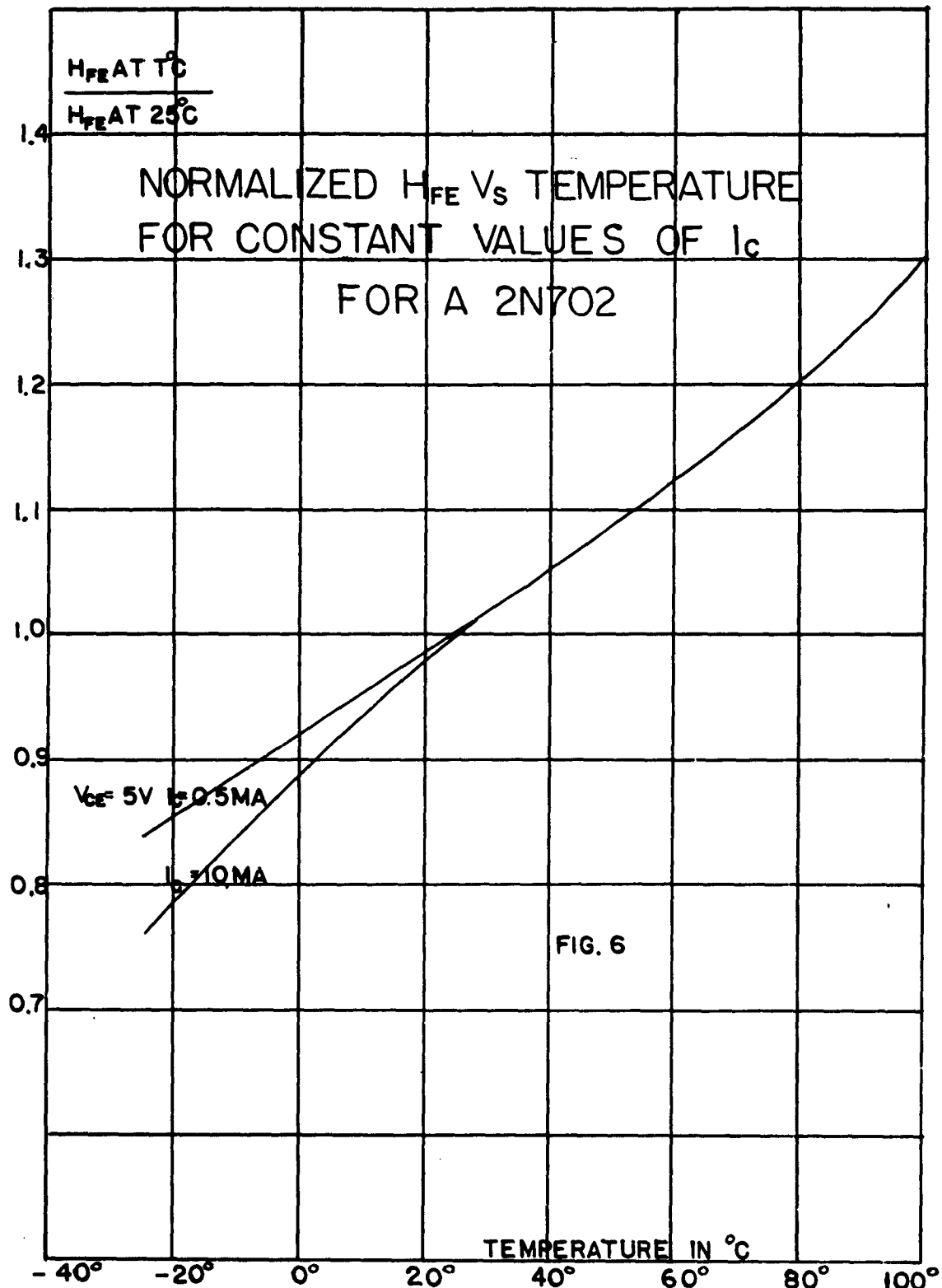
80

70 $V_{CE} = 5V$ $I_c = 20\,MA$

$I_c = 10\,MA$

60

$I_c = 5\,MA$

50

$I_c = 2\,MA$
$I_c = 1\,MA$
40 $I_c = 0.5\,MA$

FIG. 2

30

D.C. CURRENT GAIN vs. TEMPERATURE
FOR CONSTANT VALUES
OF COLLECTOR CURRENT

20

EXPERIMENTAL HOFFMAN TRANSISTOR No. 608

10 TEMPERATURE IN °C

-40°   -20°   0°   20°   40°   60°   80°   100°

8

FIG.3

D.C. CURRENT GAIN Vs TEMPERATURE
FOR CONSTANT VALUES OF
COLLECTOR CURRENT FOR A 2N702

9

$$\frac{H_{FE} \text{ AT T}^{\circ}\text{C}}{H_{FE} \text{ AT } 25^{\circ}\text{C}}$$

NORMALIZED H_{FE} V_S TEMPERATURE FOR CONSTANT VALUES OF I_c

FIG. 4

V_{CE} = 5V I_c = 0.5 MA

I_c = 20 MA

EXPERIMENTAL HOFFMAN TRANSISTOR No. 607

TEMPERATURE IN °C

-40°   -20°   0°   20°   40°   60°   80°   100°

1.4 1.3 1.2 1.1 1.0 0.9 0.8 0.7

$$\frac{H_{FE} \text{ AT } T°C}{H_{FE} \text{ AT } 25°C}$$

NORMALIZED H_{FE} V_S TEMPERATURE
FOR CONSTANT VALUES OF I_C

FIG. 5

$V_{CE} = 5V$ $I_C = 0.5 MA$

$I_C = 2.0 MA$

EXPERIMENTAL HOFFMAN TRANSISTOR No 608

TEMPERATURE IN °C

-40°   -20°   0°   20°   40°   60°   80°   10

$$\frac{H_{FE}\,AT\,T^{\circ}C}{H_{FE}\,AT\,25^{\circ}C}$$

NORMALIZED H_{FE} Vs TEMPERATURE
FOR CONSTANT VALUES OF I_C
FOR A 2N702

V_{CE}= 5V I_C=0.5MA

I_C=10MA

FIG. 6

TEMPERATURE IN °C

- 40°   -20°   0°   20°   40°   60°   80°   100°

FIG. 7 MAGNIFIED VIEW OF PHYSICAL STRUCTURE OF EXPERIMENTAL
TANTALUM WIRE OPERATIVE TRANSISTOR.

DIODE

BASE BINDING POST

EMITTER BINDING POST
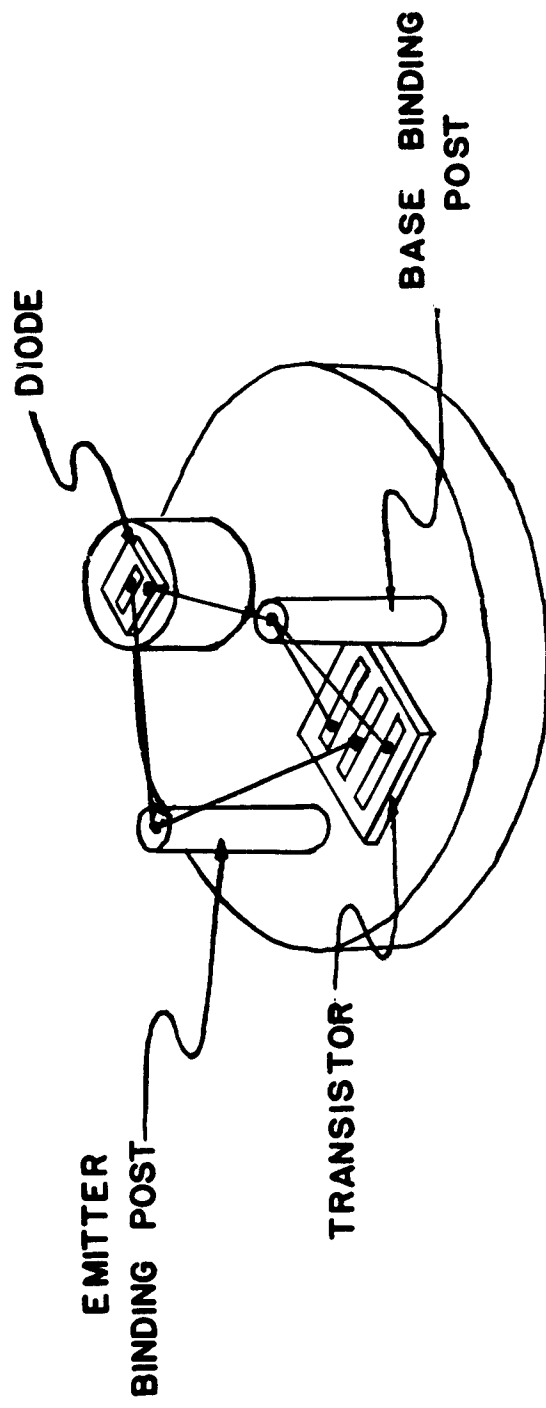
TRANSISTOR

FIG. 8 AN ISOMETRIC PICTORIAL OF THE EXPERIMENTAL HOFFMAN TEMPERATURE INSENSITIVE TRANSISTOR

14

SLOPE CONSTANT m AS A FUNCTION OF THE RATIO η

OF BASE CURRENTS FROM THE TYPE m = 2 TO m = 1

Fig. 9

2 - 33

15
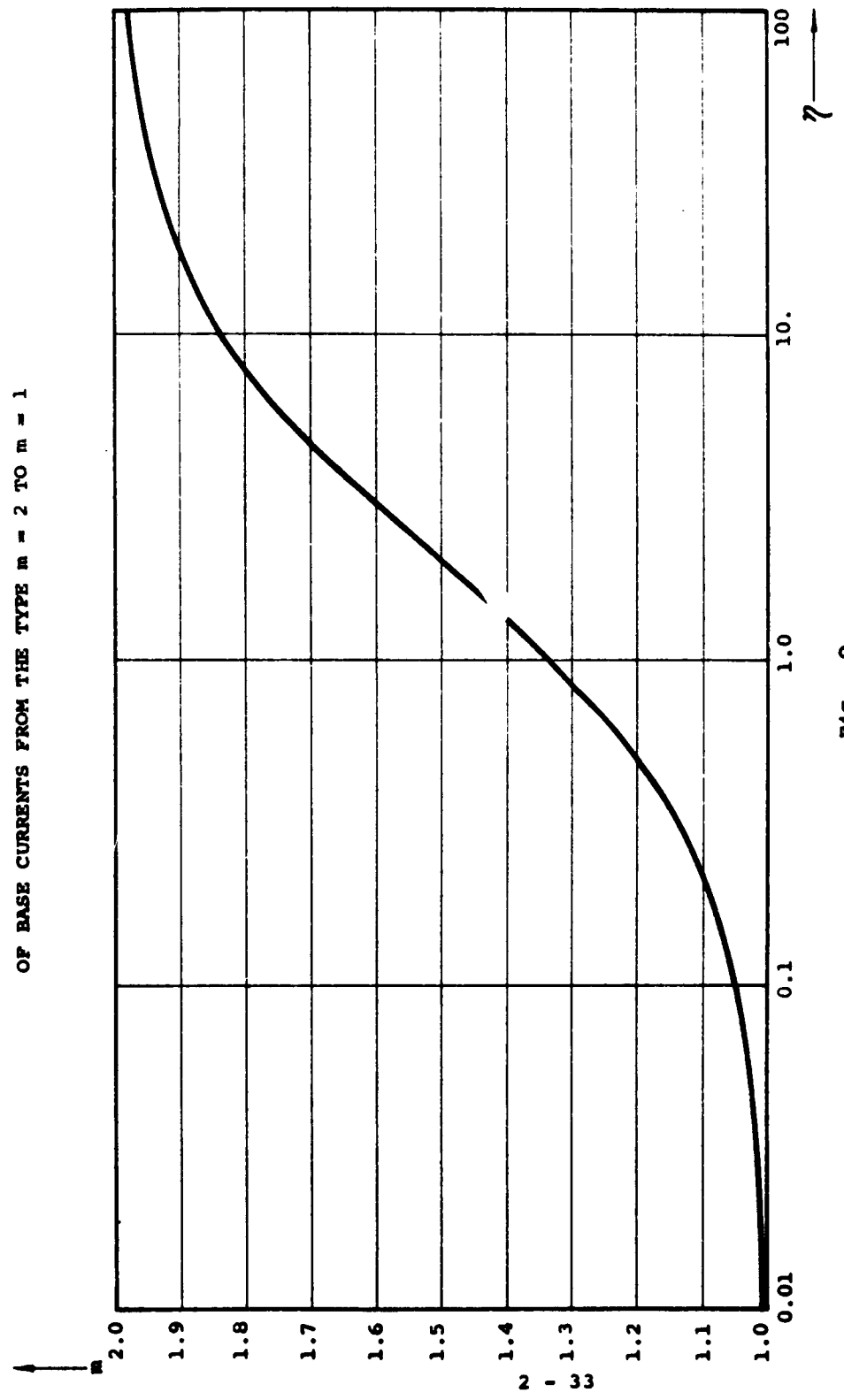
SLOPE CONSTANT m AS A FUNCTION OF THE RATIO η

OF BASE CURRENTS FROM THE TYPE m = 2 TO m = 1

Fig. 10

5 - 46

16
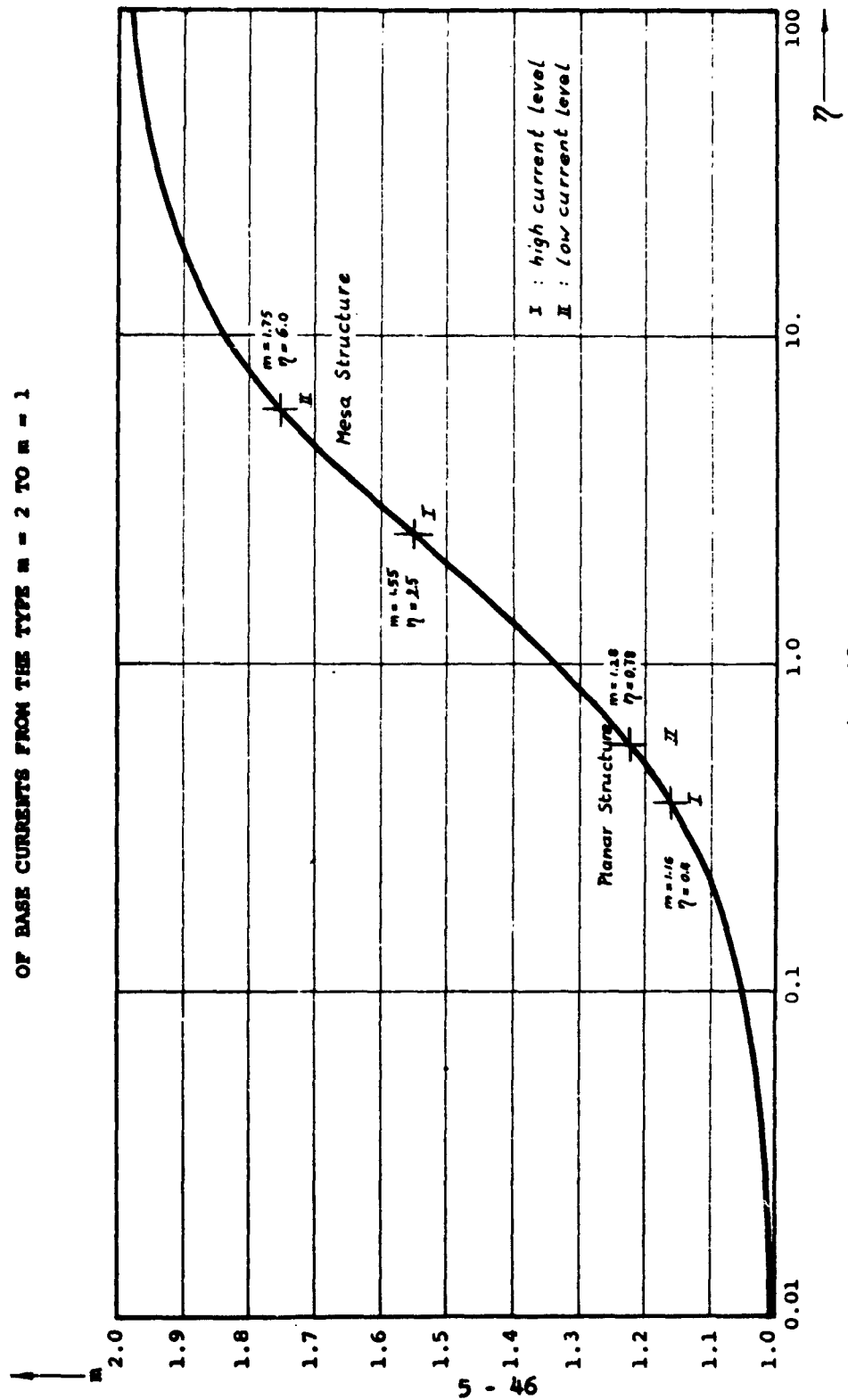
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1. Reliability
2. Transistor Devices
3. Transistor Thermal Characteristics

I. Brayden, Richard L.
II. Army Electronics Research and Development Laboratory, Fort Monmouth, N. J.
III. DA Task Nr 3A99-21-003-01

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A METHOD OF BASIC TEMPERATURE COMPENSATION IN TRANSISTORS by Richard L. Brayden, February 1963, 18 p. incl illus., 1 ref. (USAELRDL Technical Report 2311) DA Task 3A99-21-003-01) Unclassified Report

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